



CDK-2/8 Low Cost CobraNet™ Interface Module

Preliminary Data Sheet

General Description

The CDK-2 and CDK-8 are low cost CobraNet interface modules that provide hardware developers with a simple and cost effective means of adding CobraNet audio networking capabilities to their products. The CDK-2 and CDK-8 support 2 and 8 bi-directional audio channels respectively. Both are available with and without user programmable DSP processing, and with and without an HMI port connector.

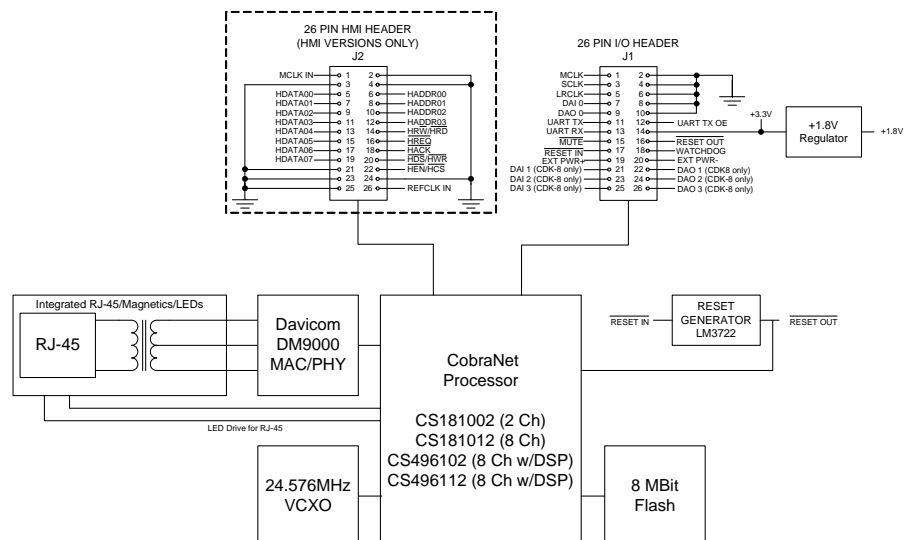
Applications

- Powered loudspeakers
- Multi-channel paging systems
- Security systems
- Two-channel and multi-channel power amplifiers
- Residential multi-zone audio networking

Features

- 100BASE-Tx, 100 Mbps, full duplex Ethernet, fully compliant with IEEE 802.3u
- Support for 48/96kHz sampling rates at up to 24 bits
- Serial bridging supported for transmission of control and metadata over the audio network
- High quality, low jitter clock source
- SNMP agent for control, monitoring, and management
- TFTP support for firmware updates over the network
- Can be powered through the RJ-45 jack (external regulation required)
- Status LEDs for Link, Activity, and CobraNet conductor
- Compact 3" x 3" form factor (3" x 3.5" w/HMI support)

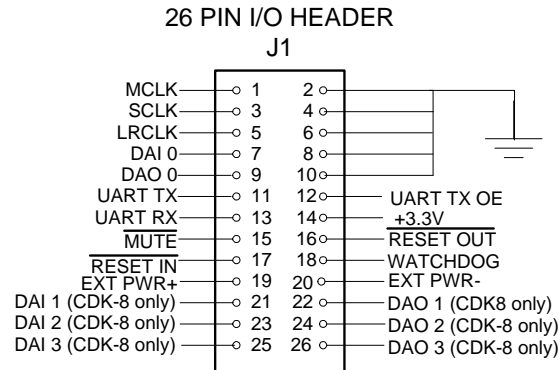
CDK-2/8 Block Diagram



CobraNet is a trademark of Cirrus Logic, Inc.

J1 and J2 (HMI Versions Only) Pin Descriptions

On CDK-2/8 modules without HMI support, all connectivity to the module is available on the 26-pin .1" female header, J1.



Pin	Signal	Direction	Notes
1	MCLK	OUT	24.576 MHz Master Audio Clock
2	GND	GND	GND
3	SCLK	OUT	Serial Audio Bit Clock (64 FS)
4	GND	GND	GND
5	LRCLK	OUT	Audio Word Clock (FS)
6	GND	GND	GND
7	DAI 0	IN	I2S Synchronous Serial Audio Data Input (CDK-2, CDK-8 - Ch 1 &2)
8	GND	GND	GND
9	DAO 0	OUT	I2S Synchronous Serial Audio Data Output (CDK-2, CDK-8 - Ch 1 &2)
10	GND	GND	GND
11	UART TX	OUT	Asynchronous Serial Transmit Data
12	UART TX OE	OUT	Asynchronous Serial Transmit Output Enable
13	UART RX	IN	Asynchronous Serial Receive Data
14	+3.3V	IN	+3.3V
15	~MUTE	OUT	Active low during initialization and when faults are detected
16	~RESET OUT	OUT	Active low reset signal generated by the CDK-2 module
17	~RESET IN	IN	Active low reset signal generated by external circuitry
18	WATCHDOG	OUT	Toggles at 750 Hz indicating proper operation. If the period exceeds 200ms, this indicates hardware or software malfunction and the module needs to be reset.

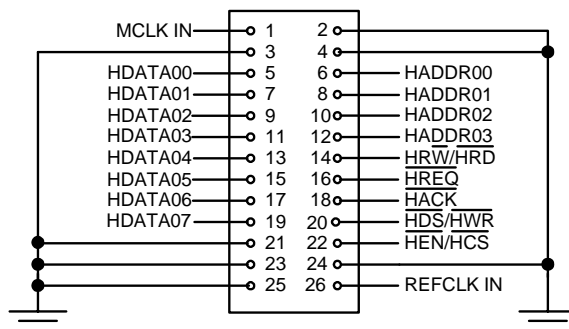
19	EXT PWR+	OUT	Connected to unused pair on RJ-45. Can be used to remotely power device connected to header. (Positive)
20	EXT PWR-	OUT	Connected to unused pair on RJ-45. Can be used to remotely power device connected to header. (Negative)
21	DAI 1	IN	I2S Synchronous Serial Audio Data Input CDK-2 = Not used CDK-8 = Channels 3 & 4
22	DAO 1	OUT	I2S Synchronous Serial Audio Data Output CDK-2 = Not used CDK-8 = Channels 3 & 4
23	DAI 2	IN	I2S Synchronous Serial Audio Data Input CDK-2 = Not used CDK-8 = Channels 5 & 6
24	DAO 2	OUT	I2S Synchronous Serial Audio Data Output CDK-2 = Not used CDK-8 = Channels 5 & 6
25	DAI 3	IN	I2S Synchronous Serial Audio Data Input CDK-2 = Not used CDK-8 = Channels 7 & 8
26	DAO 3	OUT	I2S Synchronous Serial Audio Data Output CDK-2 = Not used CDK-8 = Channels 7 & 8

The format of the synchronous serial audio interface can be changed with customized firmware. The formats supported are I²S, Cirrus Standard Mode and Normal Mode.

On CDK-2/8 modules with HMI support, the additional connector J2 is available to support connection of the Host Management Interface port to a host microcontroller.

26 PIN HMI HEADER
(HMI VERSIONS ONLY)

J2



Pin	Signal	Direction	Notes
1	MCLK IN	IN	For systems featuring multiple CobraNet interfaces operating off a common master clock.
2	GND	GND	GND
3	GND	GND	GND
4	GND	GND	GND
5	HDATA00	IN/OUT	Host Port Data (LSB)
6	HADDR00	IN	Host Port Address (LSB)
7	HDATA01	IN/OUT	Host Port Data
8	HADDR01	IN	Host Port Address
9	HDATA02	IN/OUT	Host Port Data
10	HADDR02	IN	Host Port Address
11	HDATA03	IN/OUT	Host Port Data
12	HADDR03	IN	Host Port Address (MSB)
13	HDATA04	IN/OUT	Host Port Data
14	~HRW/~HRD	IN	~HRW - Host port transfer direction (Motorola mode) ~HRD - Host Read (Intel mode)
15	HDATA05	IN/OUT	Host Port Data
16	~HREQ	OUT	Host port data request
17	HDATA06	IN/OUT	Host Port Data
18	~HACK	OUT	Host port interrupt request
19	HDATA07	IN/OUT	Host Port Data (MSB)
20	~HDS/~HWR	IN	~HDS – Host port strobe (Motorola mode) ~HWR – Host write (Intel mode)
21	GND	GND	GND
22	~HEN/~HCS	IN	~HEN – Host port enable ~HCS – Select (Intel mode)
23	GND	GND	GND
24	GND	GND	GND
25	GND	GND	GND

26	REFCLK IN	IN	Clock input for synchronizing network to an external clock source, for redundancy control and synchronization of FS divider chain to external source.
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All logic levels are 3.3V, but inputs are 5V tolerant. However, every effort should be made to use 3.3V logic signals into the CDK-2/8.

Digital Audio Timing Diagrams

There are four synchronous serial input and output interfaces coming from the CDK module. Each interface contains two channels in one sample period of the LRCLK audio word clock. The following diagram shows the timing characteristics. The characteristics are the same at both 48kHz and 96kHz sample rates. The CDK-2 module only uses the first synchronous serial interface, while all others are unused. The CDK-8 supports all 4 serial interfaces.

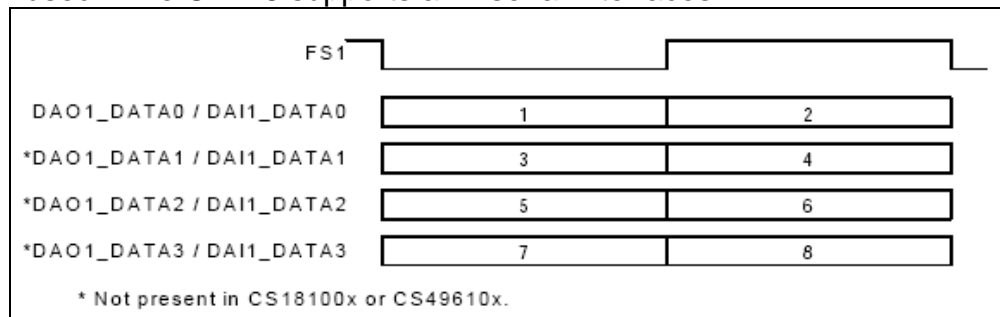


Figure 1 - Channel Structure for Synchronous Serial Audio at 64FS (One Sample Period)

Default channel ordering is shown above. Note that the first channel always begins after the rising or falling edge of FS1 (depending on the mode). DAI1_SCLK period depends on the sample rate selected. Up to 32 significant bits are received and buffered by the module for synchronous inputs. Up to 32 significant bits are transmitted by the module for synchronous outputs. Bit 31 is always the most significant (sign) bit. A 16-bit audio source must drive to bit periods 31-16 with audio data and bits 15-0 should be actively driven with either a dither signal or zeros. Cirrus Logic recommends driving unused LS bits to zero. Although data is always transmitted and received with a 32-bit resolution by the synchronous serial ports, the resolution of the data transferred to/from the Ethernet may be less. Incoming audio data is truncated to the selected resolution. Unused least significant bits on outgoing data is zero filled.

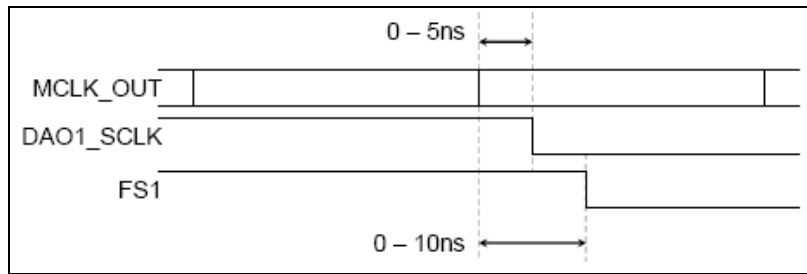


Figure 2 - Timing Relationship between FS512_OUT, DAO1_SCLK and FS1

A DAO1_SCLK edge follows an MCLK_OUT edge by 0.0 to 5.0ns. An FS1 edge follows a MCLK_OUT edge by 0.0 to 10.0ns.

Note: The DAO1_SCLK and FS1 might be synchronized with the either the falling edge or the rising edge of MCLK_OUT. Which edge is impossible to predict since it depends on power up timing.

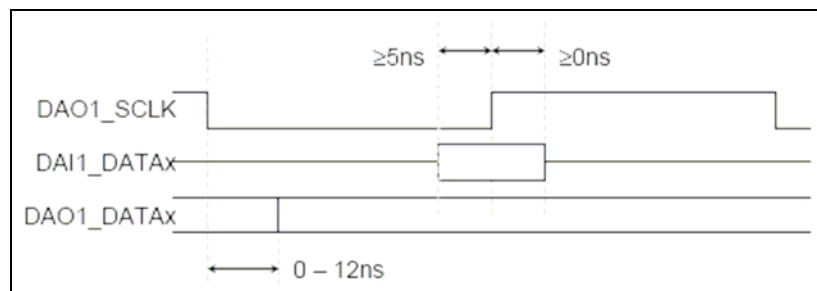


Figure 3 - Serial Port Data Timing Overview

Setup times for DAI1_DATAx and FS1 are 5.0 ns with a hold time of 0.0 ns with respect to the DAI1_SCLK edge. Clock to output times for DAO1_DATAx is 0.0 to 12.0 ns from the edge of DAO1_SCLK.

Normal Mode Data Timing

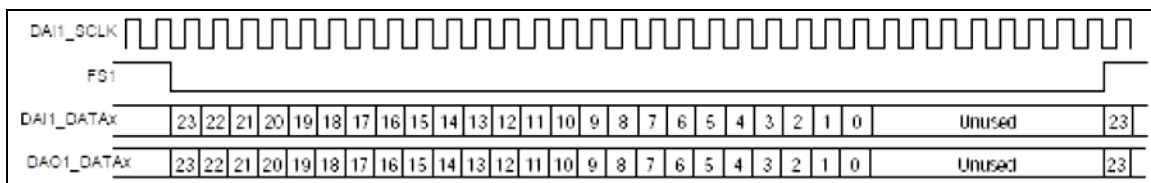


Figure 4 - Audio Data Timing Detail - Normal Mode, 64FS

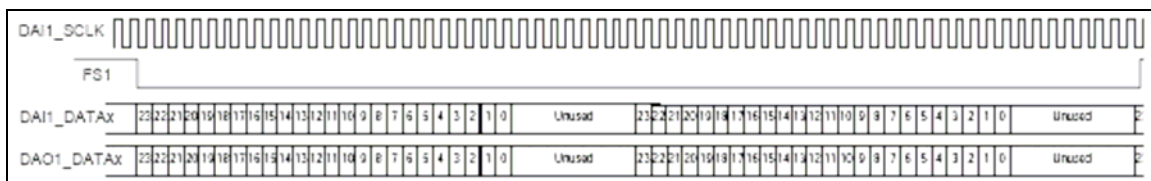


Figure 5 - Audio Data Timing Detail - Normal Mode, 128FS

Each audio channel is comprised of 32 bits of data, regardless of audio sample size. The figure above shows 24-bit audio data. The MSB is left justified and is

aligned with FS1. Data is sampled on the rising edge of DAI_SCLK and data changes on the falling edge.

I²S Mode Data Timing

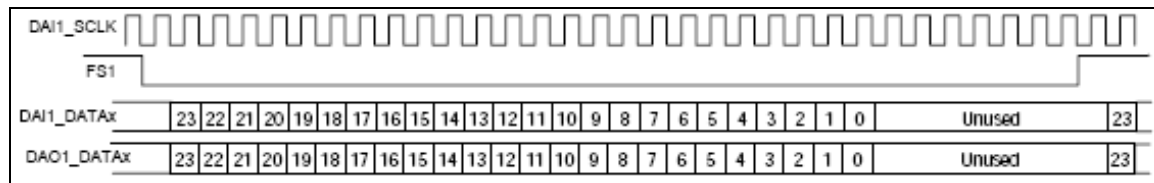


Figure 6 - Audio Data Timing Detail - I2S Mode, 64FS

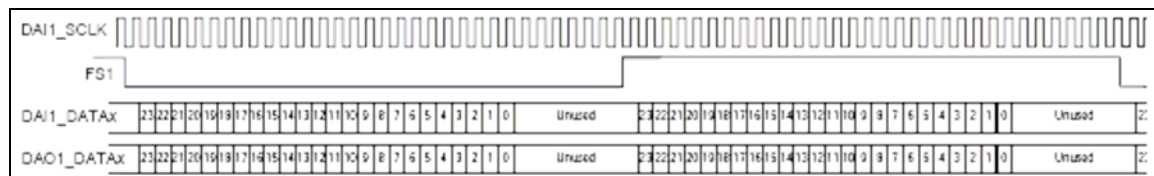


Figure 7 - Audio Data Timing Detail - I2S Mode, 128FS

Each audio channel is comprised of 32 bits of data, regardless of audio sample size. The figure above shows 24-bit audio data. The MSB is left justified and arrives one bit period following FS1. Data is sampled on the rising edge of DAI_SCLK and data changes on the falling edge.

Standard Mode Data Timing

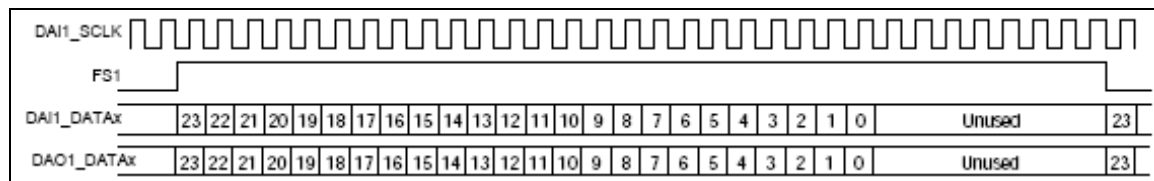


Figure 8 - Audio Data Timing Detail - Standard Mode, 64FS

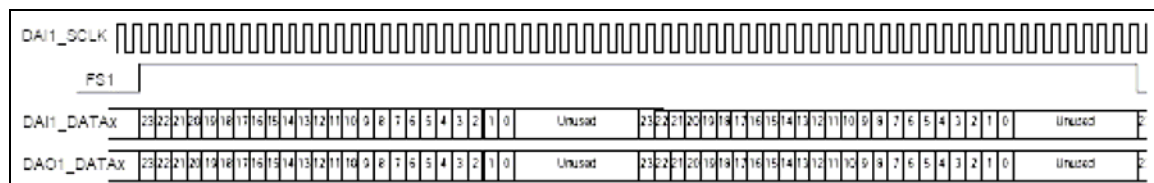


Figure 9 - Audio Data Timing Detail - Standard Mode, 128FS

Each audio channel is comprised of 32 bits of data, regardless of audio sample size. The figure above shows 24-bit audio data. The MSB is left justified and is aligned with FS1. Data is sampled on the rising edge of DAI_SCLK and data changes on the falling edge.

Host Port Interface Timing Diagrams

Motorola Mode

(C_L = 20 pF)

Parameter	Symbol	Min	Max	Unit
Address setup before $\overline{\text{HEN}}$ and $\overline{\text{HDS}}$ low	t_{mas}	5	-	ns
Address hold time after $\overline{\text{HEN}}$ and $\overline{\text{HDS}}$ low	t_{mah}	5	-	ns
Read				
Delay between $\overline{\text{HDS}}$ then $\overline{\text{HEN}}$ low or $\overline{\text{HEN}}$ then $\overline{\text{HDS}}$ low	t_{modr}	0	-	ns
Data valid after $\overline{\text{HEN}}$ and $\overline{\text{HDS}}$ low with $\text{HR}\overline{\text{W}}$ high	t_{mdd}	-	19	ns
$\overline{\text{HEN}}$ and $\overline{\text{HDS}}$ low for read	t_{mrpw}	24	-	ns
Data hold time after $\overline{\text{HEN}}$ or $\overline{\text{HDS}}$ high after read	t_{mdhr}	8	-	ns
Data high-Z after $\overline{\text{HEN}}$ or $\overline{\text{HDS}}$ high after read	t_{mdis}	-	18	ns
$\overline{\text{HEN}}$ or $\overline{\text{HDS}}$ high to $\overline{\text{HEN}}$ and $\overline{\text{HDS}}$ low for next read	t_{mrd}	30	-	ns
$\overline{\text{HEN}}$ or $\overline{\text{HDS}}$ high to $\overline{\text{HEN}}$ and $\overline{\text{HDS}}$ low for next write	t_{mrdtw}	30	-	ns
$\text{HR}\overline{\text{W}}$ rising to HREQ falling	t_{mrwirqh}	-	12	ns
Write				
Delay between $\overline{\text{HDS}}$ then $\overline{\text{HEN}}$ low or $\overline{\text{HEN}}$ then $\overline{\text{HDS}}$ low	t_{modw}	0	-	ns
Data setup before $\overline{\text{HEN}}$ or $\overline{\text{HDS}}$ high	t_{mdsu}	8	-	ns
$\overline{\text{HEN}}$ and $\overline{\text{HDS}}$ low for write	t_{mwpw}	24	-	ns
$\text{HR}\overline{\text{W}}$ setup before $\overline{\text{HEN}}$ and $\overline{\text{HDS}}$ low	t_{mrwsu}	24	-	ns
$\text{HR}\overline{\text{W}}$ hold time after $\overline{\text{HEN}}$ or $\overline{\text{HDS}}$ high	t_{mrwhld}	8	-	ns
Data hold after $\overline{\text{HEN}}$ or $\overline{\text{HDS}}$ high	t_{mdhw}	8	-	ns
$\overline{\text{HEN}}$ or $\overline{\text{HDS}}$ high to $\overline{\text{HEN}}$ and $\overline{\text{HDS}}$ low with $\text{HR}\overline{\text{W}}$ high for next read	t_{mwtrd}	30	-	ns
$\overline{\text{HEN}}$ or $\overline{\text{HDS}}$ high to $\overline{\text{HEN}}$ and $\overline{\text{HDS}}$ low for next write	t_{mwd}	30	-	ns
$\text{HR}\overline{\text{W}}$ rising to HREQ falling	t_{mrwbsyl}	-	12	ns

NOTES:1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the HREQ pin/bit should be observed to prevent overflowing the input data buffer.

Figure 10 – Host Port Timing Relationships – Motorola Mode

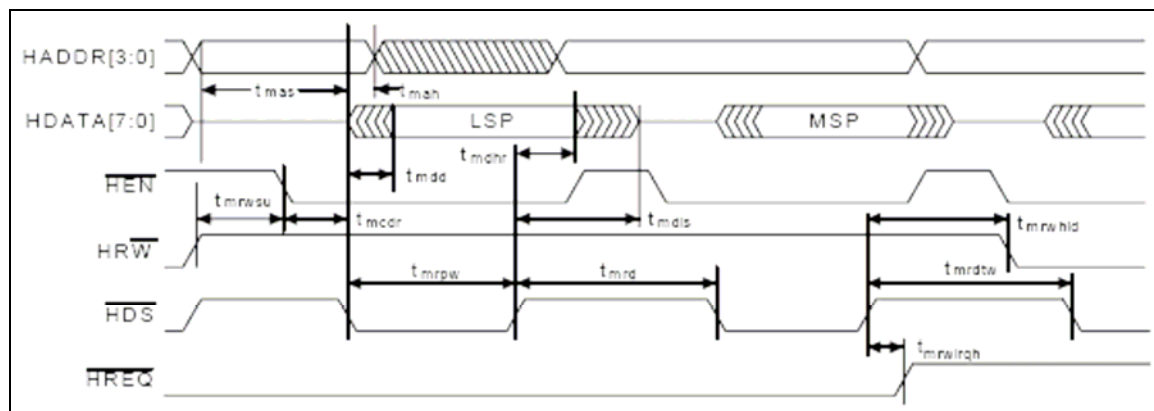


Figure 11 – Host Port Read Cycle Timing – Motorola Mode

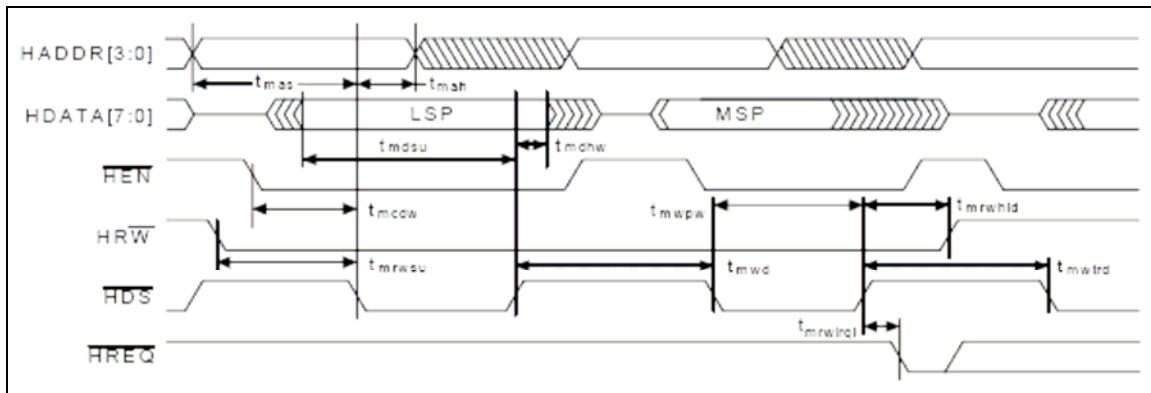


Figure 12 – Host Port Write Cycle Timing – Motorola Mode

Intel Mode

(C _L = 20 pF)				
Parameter	Symbol	Min	Max	Unit
Address setup before $\overline{\text{HCS}}$ and $\overline{\text{HRD}}$ low or $\overline{\text{HCS}}$ and $\overline{\text{HWR}}$ low	t_{ias}	5	-	ns
Address hold time after $\overline{\text{HCS}}$ and $\overline{\text{HRD}}$ low or $\overline{\text{HCS}}$ and $\overline{\text{HWR}}$ high	t_{iah}	5	-	ns
Read				
Delay between $\overline{\text{HRD}}$ then $\overline{\text{HCS}}$ low or $\overline{\text{HCS}}$ then $\overline{\text{HRD}}$ low	t_{icdr}	0	-	ns
Data valid after $\overline{\text{HCS}}$ and $\overline{\text{HRD}}$ low	t_{idd}	-	18	ns
$\overline{\text{HCS}}$ and $\overline{\text{HRD}}$ low for read	t_{irpw}	24	-	ns
Data hold time after $\overline{\text{HCS}}$ or $\overline{\text{HRD}}$ high	t_{idhr}	8	-	ns
Data high-Z after $\overline{\text{HCS}}$ or $\overline{\text{HRD}}$ high	t_{idis}	-	18	ns
$\overline{\text{HCS}}$ or $\overline{\text{HRD}}$ high to $\overline{\text{HCS}}$ and $\overline{\text{HRD}}$ low for next read	t_{ird}	30	-	ns
$\overline{\text{HCS}}$ or $\overline{\text{HRD}}$ high to $\overline{\text{HCS}}$ and $\overline{\text{HWR}}$ low for next write	t_{irdtw}	30	-	ns
$\overline{\text{HRD}}$ rising to $\overline{\text{HREQ}}$ rising	$t_{irdirghl}$	-	12	ns
Write				
Delay between $\overline{\text{HWR}}$ then $\overline{\text{HCS}}$ low or $\overline{\text{HCS}}$ then $\overline{\text{HWR}}$ low	t_{icdw}	0	-	ns
Data setup before $\overline{\text{HCS}}$ or $\overline{\text{HWR}}$ high	t_{idsu}	8	-	ns
$\overline{\text{HCS}}$ and $\overline{\text{HWR}}$ low for write	t_{iwpw}	24	-	ns
Data hold after $\overline{\text{HCS}}$ or $\overline{\text{HWR}}$ high	t_{idhw}	8	-	ns
$\overline{\text{HCS}}$ or $\overline{\text{HWR}}$ high to $\overline{\text{HCS}}$ and $\overline{\text{HRD}}$ low for next read	t_{iwdtd}	30	-	ns
$\overline{\text{HCS}}$ or $\overline{\text{HWR}}$ high to $\overline{\text{HCS}}$ and $\overline{\text{HWR}}$ low for next write	t_{iwd}	30	-	ns
$\overline{\text{HWR}}$ rising to $\overline{\text{HREQ}}$ falling	$t_{iwrbsyl}$	-	12	ns
NOTES:1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the $\overline{\text{HREQ}}$ pin/bit should be observed to prevent overflowing the input data buffer.				

Figure 13 – Host Port Timing Relationships – Intel Mode

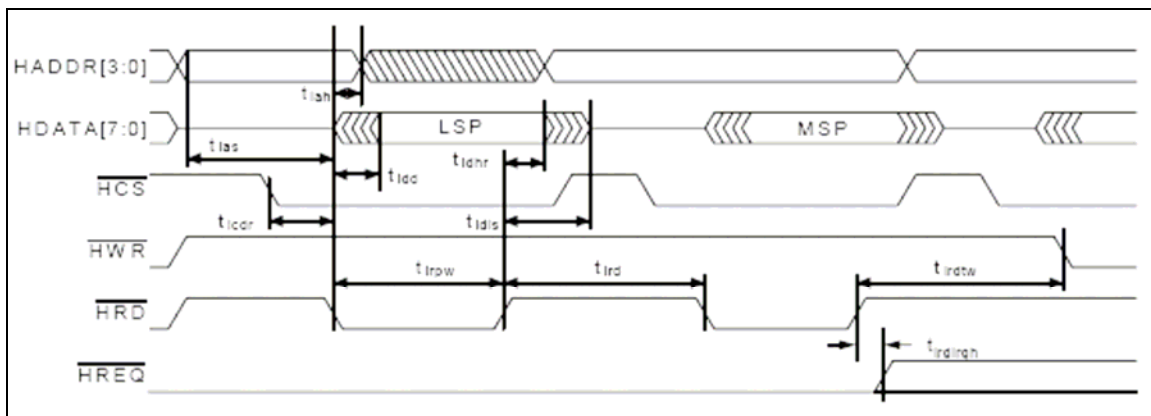


Figure 14 – Host Port Read Cycle Timing – Intel Mode

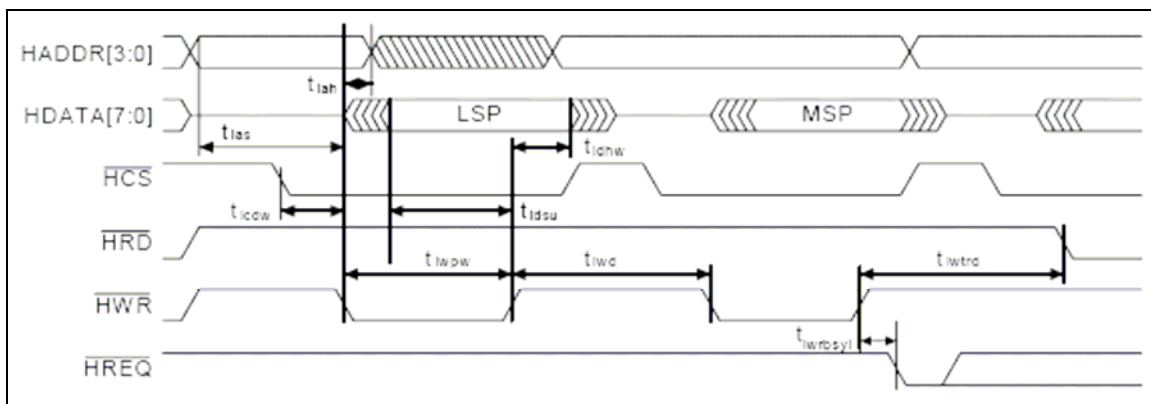
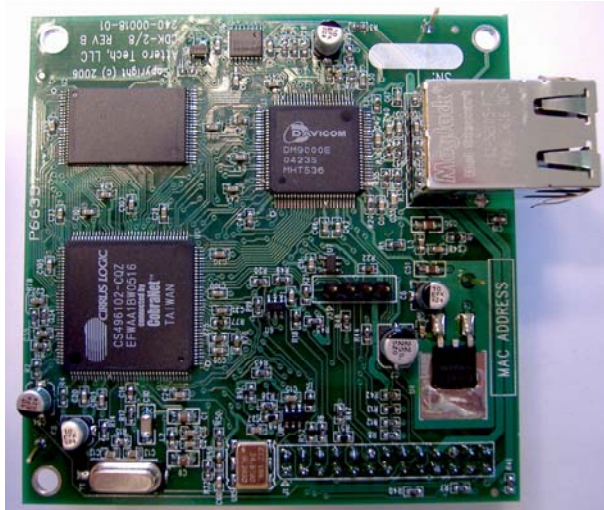


Figure 15 – Host Port Write Cycle Timing – Intel Mode

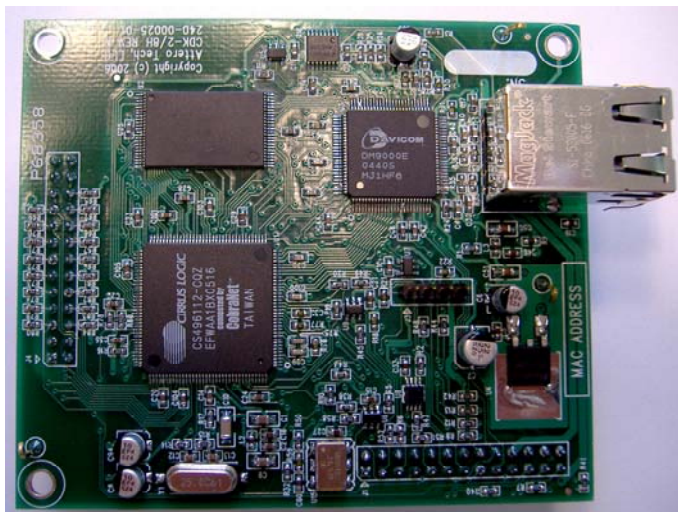
Power Requirements

The CDK-2/8 requires a regulated +3.3V DC supply at 600 mA. Power consumption is approximately 2W.

Module Photographs

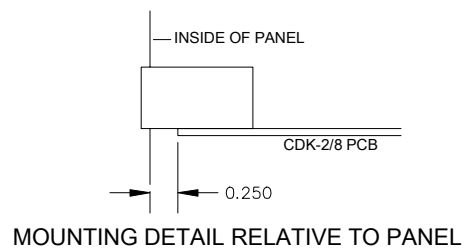
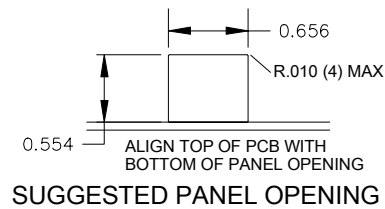
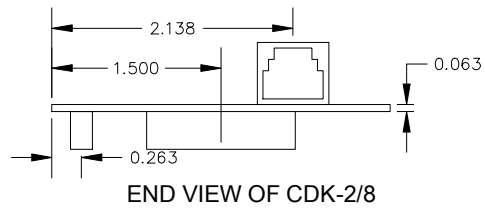
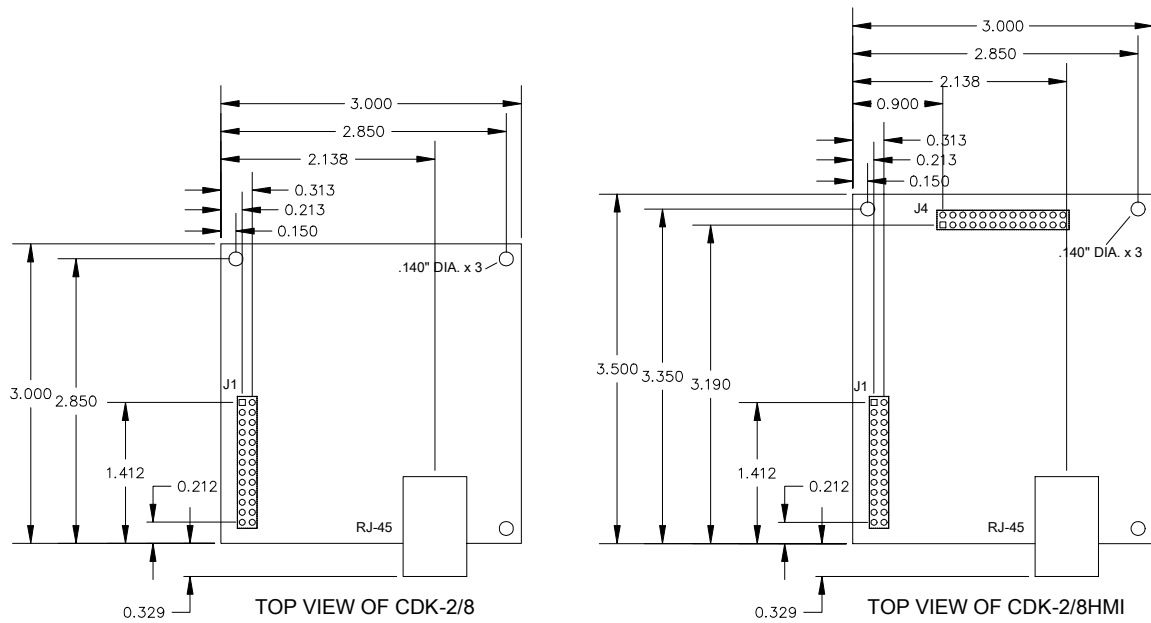


CDK-2/8



CDK-2/8HMI

Mechanical Outlines



Applications Information

Basic Bring-up

The CDK-2/8 module is preloaded with the most up to date CobraNet firmware. Basic functionality can be tested, before integrating into the target product, by applying a regulated and current limited +3.3V power supply between J1 pin 14 (+3.3V) and J1 pin 10 (Gnd).

Follow these steps to verify functionality:

- Connect a CAT-5 Ethernet cable between an Ethernet switch and the RJ-45 connector on the CDK-2/8
- Connect a PC to the same Ethernet switch
- Apply power to the CDK-2/8
- Assign a static IP address to your network interface card on the PC
- Start the CobraNet Discovery¹ application

You can now monitor and manipulate the CDK-2/8 module using the CobraNet Discovery application. Connecting another CobraNet device to the same network will allow audio and data transmission to be configured between the devices.

Integration Tips

The CDK modules have been designed for easy integration into other products. The only connection required between the CDK-2/8 and the target hardware is the mating 26-pin .1" header.

All the serial audio signals and clock signals include either 22 ohm series termination resistors or buffers located near J1. If the clock and audio traces are long or have multiple loads you may consider adding additional series termination resistors or buffers to ensure clean signals.

It is also recommended that bypass capacitors be placed near +3.3V(pin 12) to reduce the AC signal return path. A 0.1uF capacitor in parallel with a 10uf-47uf electrolytic between +3.3V and ground is suggested.

Software Tools

There are a number of CobraNet software tools available to assist in the development, control and maintenance of CobraNet enabled products. All software is available from Cirrus Logic at www.cirrus.com/cobranetsoftware.

- CobraNet Discovery – Monitoring and Firmware Updates
- CNCustom – Firmware Customization Utility

¹ CobraNet Discovery is provided by Cirrus Logic at www.cirrus.com/cobranetsoftware

- CobraCAD – CobraNet network design tool
- DSP Conductor – Drag and Drop DSP configuration software

Firmware Updates

Each CDK-2/8 is preloaded with the most current version of CobraNet firmware with customizations. If a newer version is released after receiving the CDK-2/8 module, the updated CobraNet firmware can be downloaded from Cirrus Logic.

It is important to remember that the initial firmware is customized, any new firmware versions will be generic CobraNet versions and may affect the interface between the CDK-2/8 and the hardware it resides in. In particular, all generic versions of CobraNet firmware set the serial audio format to Normal mode. The CDK-2/8 firmware is set for I2S mode. It is recommended that CNCustom, a tool for customizing generic CobraNet firmware, be used to create unique firmware versions for your end product.

Attero Tech will provide the most current CDK-2/8 module firmware upon request.

Ordering Information

Part Number	Description
CDK-2	2 Channel Interface, no user DSP
CDK-2D	2 Channel Interface with user DSP
CDK-8	8 Channel Interface, no DSP
CDK-8D	8 Channel Interface with user DSP
CDK-2HMI	2 Channel Interface w/HMI port, no user DSP
CDK-2DHMI	2 Channel Interface w/HMI port and user DSP
CDK-8HMI	8 Channel Interface w/HMI port, no user DSP
CDK-8DHMI	8 Channel Interface w/HMI port and user DSP